

12-29-99

Attorney Docket No. P992062

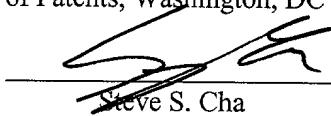
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**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

**CERTIFICATE OF EXPRESS MAILING**

I hereby certify that this paper and the documents and/or fees referred to as attached therein are being deposited with the United States Postal Service on December 28, 1999 in an envelope as "Express Mail Post Office to Addressee" service under 37 CFR § 1.10, Mailing Label Number EJ 706598878 US, addressed to Assistant Commissioner of Patents, Washington, DC 20231.

  
Steve S. Cha

**UTILITY PATENT APPLICATION TRANSMITTAL (37 CFR § 1.53(b))**

Assistant Commissioner for Patents  
Box Patent Application  
Washington, D.C. 20231

Transmitted herewith for filing is the patent application under 37 CFR § 1.53(b) in the name of inventor(s) of:

Seung-Hwan Oh

For: METHOD FOR PROCESSING ERROR OF RECEIVED PACKET IN ETHERNET MAC LAYER

Enclosed are:

Application Elements:

- 2 copies each of 3 sheets of informal drawing(s).
- Assignment of the invention to: SAMSUNG ELECTRONIC CO., LTD.
- Specification, Claims, and Abstract: Nr. of sheets: 11
- A copy of combined declaration and power of attorney:

Accompanying Application Parts:

- A check\* 1501 in the amount of \$760.00 for filing fee
- A Return Receipt Postcard
- Assignment and Assignment Recordation Cover Sheet (recording fee of \$40.00 enclosed)

- Claim of priority under 35 U.S.C. §119 and a copy of certified Korean Patent Application.
- Information disclosure statements: Nr. of sheets: 3
- Preliminary Amendment
- Small Entity Statement(s)

The filing fee has been calculated as shown below (37 CFR §1.16):

<b>For:</b>	<b>No. Filed</b>	<b>No.Extra</b>	<b>Rate(Small Entity)</b>	<b>Fee(Small Entity)</b>
<b>Basic Fee</b>	20 claims			\$ 760.00 (\$380)
<b>Total Claims</b>	4 claims - 20 =	0	\$18(\$9)/claim	\$ 0.00
<b>Independent Claims</b>	2 claims - 3 =	0	\$78(39)/claim	\$ 0.00
<b>Multiple Dep. Claims</b>			\$130(65)/claim	\$ 0.00
			<b>Total Filing Fee</b>	<b>\$ 760.00</b>

General Authorization for Petition for Extension of Time (37 CFR §1.136)

Applicant hereby make and generally authorize any Petitions for Extensions of Time as may be needed for any subsequent filings.

Should the enclosed check become lost or detached from the file, Assistant Commissioner is authorized to charge our Deposit Account No. 50-1005 and advise the undersigned attorney accordingly. Also, should the enclosed check be deemed to be deficient or excessive in payment, the Commissioner is authorized to charge or credit our deposit account and notify the undersigned attorney of any such transaction.

In view of the above, it is respectfully requested that this application be accorded a filing date pursuant to 37 C.F.R. §1.53(b).

Mailed: December 28, 1999

  
Steve S. Cha, Registration No. 44,069  
Attorney for Applicant(s)

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**Customer No:022491**



**022491**

PATENT TRADEMARK OFFICE

**METHOD FOR PROCESSING ERROR OF RECEIVED PACKET IN ETHERNET**

**MAC LAYER**

**CLAIM OF PRIORITY**

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This application makes reference to, incorporates the same herein, and claims all benefits accruing under 35 U.S.C. Section 119 from an application for "Method for Processing Error of Received Packet in Ethernet MAC Layer" filed in the Korean Industrial Property Office on December 28, 1998 and there duly assigned Serial No. 98-59204.

10

**BACKGROUND OF THE INVENTION**

**1. Field of the Invention**

15 The present invention relates generally to a method for processing a received packet in a MAC (Medium Access Control) layer of an Ethernet, and in particular, to a method for processing an error in the received packet.

**2. Description of the Related Art**

20 A local area network (LAN) interconnects a group of data communication terminals within a limited area. This type of LAN topology is classified into bus type, ring type, star type and tree type. The bus type network is the most commonly used network,

and the Ethernet is one of the oldest communication protocols for communication terminals implemented in the bus physical topology.

Meanwhile, a MAC layer of the Ethernet processes a packet received from a physical layer. When an error occurs during the reception of data from the physical layer, the MAC layer performs the corresponding error processing operation. More specifically, when an error occurs in the packet exceeding 64 bytes while receiving the packet from the physical layer, the MAC layer receives the entire packet and transmits the received packet to the next stage along with an error signal indicating the occurrence of an error in the received packet. A MAC protocol standard and a logical link control (LLC) protocol standard, including the error processing method for the received data in the MAC layer, have been published by the IEEE (Institute of Electrical and Electronics Engineers) 802 Committee and certified by ISO (International Standard Organization).

According to the above standards, when an error occurs in the packet not exceeding 64 bytes while receiving the packet, the MAC layer will discard the error packet. However, when an error occurs in a packet exceeding 64 bytes, the MAC layer will receive the entire packet and transmit the received packet to the next stage (e.g., switch), along with an error signal indicating the occurrence of the error. Therefore, the receipt of the unnecessary error packet causes an increase in the overhead of the system. In particular, a switch in the next stage receiving the error packet wastes time by receiving the unnecessary error packet, thereby causing a degradation of the system performance.

## SUMMARY OF THE INVENTION

It is, therefore, an object of the present invention to provide a method for reducing  
5 an overhead due to the reception of error packets in an MAC layer of the Ethernet.

It is another object of the present invention to provide a method for saving the time  
wasted by receiving the unnecessary packet in a MAC layer of the Ethernet.

10 It is further another object of the present invention to provide a method for  
improving the receiving capability in a MAC layer of the Ethernet.

To achieve the above objects, there is provided a method for processing a received  
packet in a MAC (Medium Access Control) layer of an Ethernet which receives a packet  
15 from a physical layer and transmits the received packet to a switch.

In accordance with one aspect of the present invention, a method for processing a  
received packet in a MAC layer comprises the steps of detecting an error while receiving  
the packet from the physical layer; transmitting the received packet to the switch upon the  
20 failure to detect an error; and, stop the transmission of the receiving packet to the switch  
upon detecting an error.

In accordance with another aspect of the present invention, a method for processing a received packet in a MAC layer comprises the steps of receiving a packet from the physical layer and storing the received packet in the FIFO (First-In, First-Out) memory; detecting error while receiving the packet; stopping the storage of the received packet to the 5 FIFO memory upon the detection of error; and, transmitting a signal indicating the occurrence of error and a signal indicating the end of the received packet to the switch. Further, the method comprises the step of preparing to receive the next packet from the physical layer, after receiving the error packet.

10

#### **A BRIEF DESCRIPTION OF THE DRAWINGS**

The above and other objects, features and advantages of the present invention will become more apparent from the following detailed description when taken in conjunction with the accompanying drawings in which:

15 FIG. 1 is a block diagram illustrating a scheme for processing the received packet in an Ethernet MAC layer according to an embodiment of the present invention;

FIG. 2 is a state diagram illustrating a procedure for processing the received data according to the configuration shown in FIG. 1; and,

20 FIG. 3 is a timing diagram illustrating the error processing operation for a received packet which is performed in the FIFO controller of FIG. 1.

## A DETAILED DESCRIPTION OF THE PREFERRED EMBODIMENT

A preferred embodiment of the present invention will be described herein below with reference to the accompanying drawings. For the purpose of clarity, well-known 5 functions or constructions are not described in detail as they would obscure the invention in unnecessary detail.

FIG. 1 shows a configuration according to an embodiment of the present invention for processing error in a received packet in a MAC layer. The MAC layer stores the packet 10 received from a physical layer 10 in a FIFO (First-In, First-Out) memory 50 and transmits the stored packet to a switch (not shown) in the next stage through a switch engine interface 60. Such MAC layer includes a FIFO controller 20, an error controller 40, and the FIFO memory 50. The FIFO controller 20 also includes a state machine 30.

15 In FIG. 1, when the FIFO controller 20 receives a packet S2 from the physical layer 10, the error controller 40 examines whether the received packet (e.g., 4 bits) contains an error. The error controller 40 checks for a collision of the received packet, an overflow of the FIFO memory 50, and the parity and the CRC (Cyclic Redundancy Code) of the received packet, to examine whether the received packet has error. When it is determined 20 that the received packet contains error, the error controller 40 provides the FIFO controller 20 with an error signal S5. The FIFO memory 50 stores the packet received from the physical layer 10 and then transmits the stored packet to the switch engine interface 60 in

response to a control signal S3 from the FIFO controller 20. The FIFO controller 20 controls the operation of storing the packet received from the physical layer 10 in the FIFO memory 50 and then transmitting the stored packet to the switch engine interface 60, using the control signal S3. Here, an output enable signal OEN, a write enable signal WEN or a 5 chip select signal /CS can be used for the control signal S3. The state machine 30 included in the FIFO controller 20 determines the operating state of the FIFO controller 20 according to the error signal S5 from the error controller 40. In the embodiment of the present invention, the FIFO controller 20 operates in an idle state, a normal state or an error state according to the state machine 30.

10

Further, the reference letter S1 denotes a signal indicating the reception of a packet from the physical layer 10, and the reference letter S4 denotes a signal ERR indicating the occurrence of error during the receipt of the packet in the FIFO controller 20 and a signal EOP (End of Packet) indicating the completion of receiving the packet.

15

FIG. 2 is a state diagram illustrating an operating state of the FIFO controller 20, determined by the state machine 30. FIG. 3 is a timing diagram illustrating an error processing operation for the received packet which is performed in the FIFO controller 20 of FIG. 1.

20

When the error controller 40 determines that a new packet has been normally received from the physical layer 10 of FIG. 1, the FIFO controller 20 stores the received

packet in the FIFO memory 50 and then transmits the stored packet to the switch engine interface 60. When the normal packet is received normally, the S1 signal (or data valid signal) is represented by “1.” In this case, the FIFO controller 20 operates in the normal state 34.

5

However, when the error controller 40 determines that an error has occurred while transmitting the received packet to the switch engine interface 60 (i.e., when S5= “1”), the FIFO controller 20 changes to the error state 36. In this situation, the FIFO controller 20 stops transmitting the received packet to the switch engine interface 60. More specifically, 10 the FIFO controller 20 provides a chip select signal /CS of level “1”, as shown in FIG. 3, to “the FIFO memory 50 to prevent the received packet from being stored in the FIFO memory 50, and at the same time, provides the error signal ERR and the end-of-packet signal EOP to the switch engine interface 60.

15 In prior art, when an error occurs during the reception mode of the packet, the FIFO controller 20 receives the entire error packet and transmits it to the switch engine interface 60. When an error occurs at the time where the end of the packet is completely received, the FIFO controller 20 provides the switch engine interface 60 with a signal indicating the complete reception mode of the packet.

20

During the error processing operation in error state 36, upon the receipt of the S1 signal of level “0” indicating that there is no packet to be received from the physical layer

10, the FIFO controller 20 converts to the idle state 32. In the idle state 32, the FIFO controller 20 prepares to receive the next packet from the physical layer 10.

As described above, upon the receipt of an error packet from the physical layer, the

5 MAC layer discards the error packet and at the same time provides a switch in the next stage with a signal indicating the occurrence of an error. In this manner, it is possible to reduce an overhead due to the reception of the error packet in the MAC layer. In addition, it is possible to save the time wasted as a result of receiving the unnecessary packet. In summary, it is possible to improve the receiving capability in the MAC layer of the  
10 Ethernet.

While the invention has been shown and described with reference to a certain preferred embodiment thereof, it will be understood by those skilled in the art that various changes in form and details may be made therein without departing from the spirit and the

15 scope of the invention as defined by the appended claims.

**WHAT IS CLAIMED IS:**

1. A method for processing a packet received from a physical layer by a MAC (Medium Access Control) layer of an Ethernet to be transmitted to a switch, the 5 method comprising the steps of:

detecting error while receiving the packet from the physical layer;  
upon failure to detect the error, transmitting the received packet to the switch; and,  
upon detection of the error, stopping the transmission of the received packet to the switch.

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2. A method for processing a packet received from a physical layer by a MAC layer of an Ethernet, wherein the received packet is stored in a memory for an eventual transmission to a switch, the method comprising the steps of:

receiving a packet from the physical layer and storing the received packet in the 15 memory;

detecting for error while receiving the packet;  
upon detection of the error, stopping the storage of the received packet in the memory; and,

transmitting a first signal indicating an occurrence of the error and a second signal 20 indicating an end of the received packet to the switch.

3. The method as claimed in Claim 2, wherein the method further

comprising the step of preparing to receive a next packet from the physical layer after receiving the error packet.

4. The method as claimed in Claim 2, wherein said memory comprises a

5 FIFO (First-In, First-Out) memory.

## **ABSTRACT OF THE DISCLOSURE**

A method for processing a received packet in a MAC (Medium Access Control) layer of an Ethernet which receives a packet from a physical layer and  
5 transmits the received packet to a switch. The method includes the steps of detecting an error while receiving the packet from the physical layer; upon failure to detect error, transmitting the received packet to the switch; and, upon detection of error, stopping the transmission of the received packet to the switch.

FIG. 1

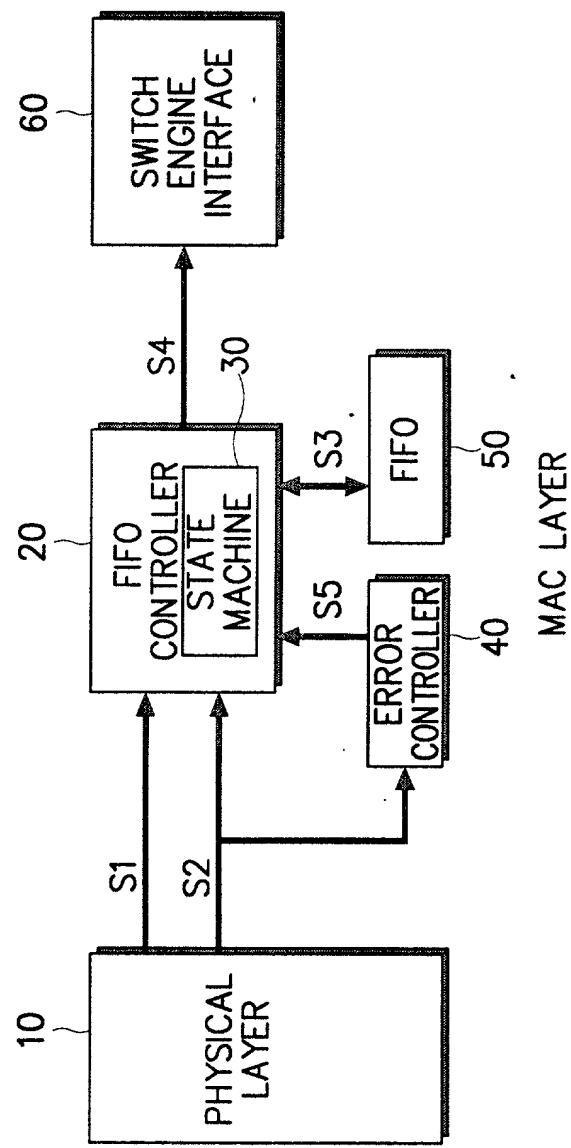


FIG. 2

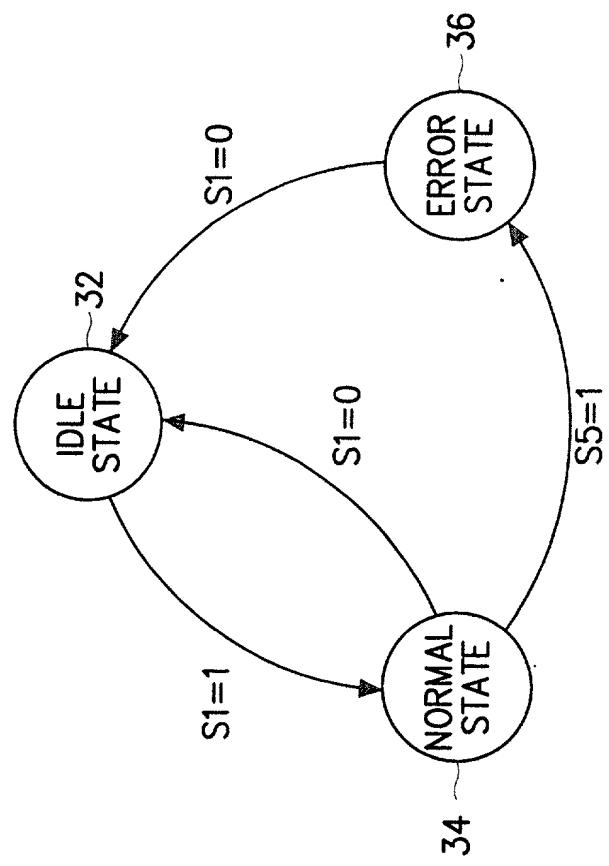
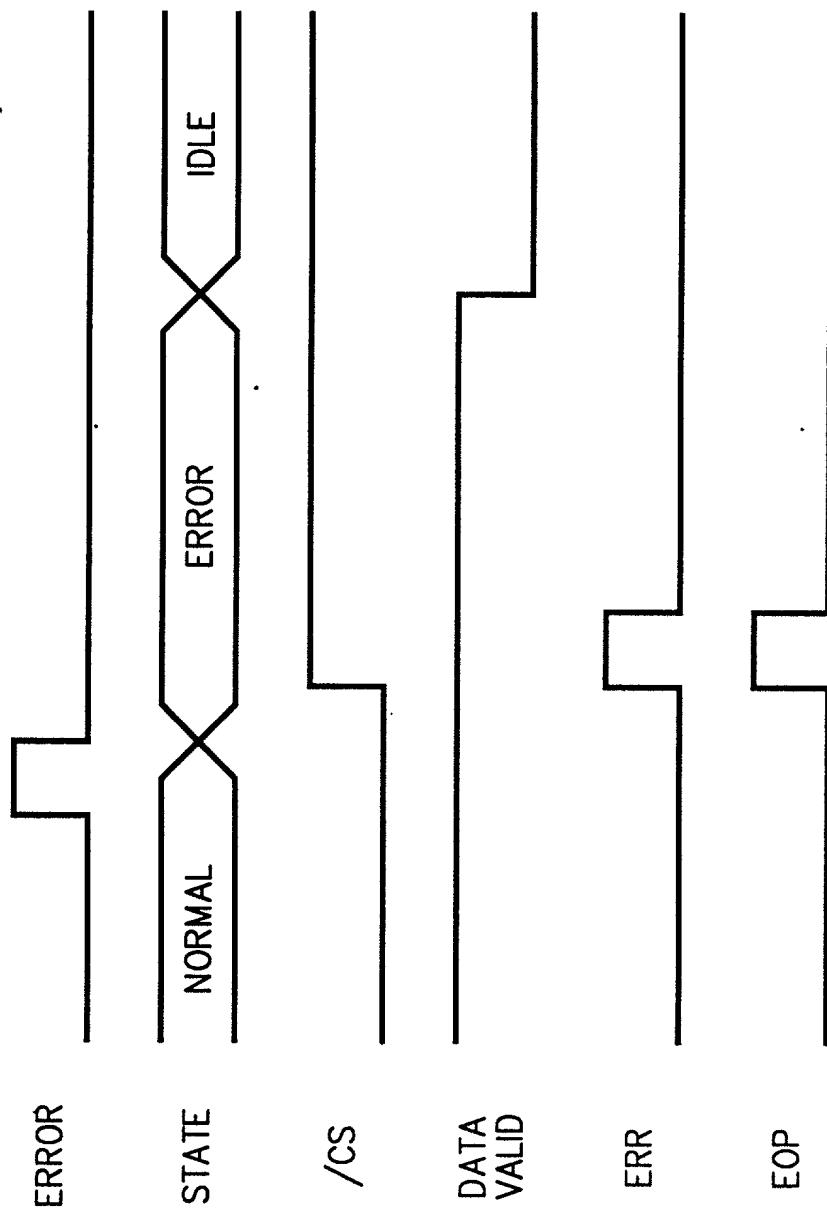


FIG. 3



**IN THE UNITED STATES PATENT AND TRADEMARK OFFICE**

In re application of: Seung-Hwan Oh

Serial No: *Not yet assigned.* Examiner: *Not yet assigned.*

Filed: December 28, 1999 Group: *Not yet assigned.*

For: METHOD FOR PROCESSING ERROR OF RECEIVED PACKET IN  
ETHERNET MAC LAYER

**TRANSMITATAL OF DECLARATION**

Assistant Commissioner for Patents  
Washington, DC 20231

Sir:

This transmittal accompanies a fax copy of Declaration with the signature by the inventors, for the above-captioned application. A substitute Declaration with the inventors' signature will be filed upon receipt of the Serial No. for the above-captioned application.

Respectfully submitted,



Steve S. Cha  
Attorney for the Applicant  
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Date: December 28, 1999

PTO/SB/02B

Customer No.:022491  
Docket No.: p992062**DECLARATION AND POWER OF ATTORNEY**

As a below named inventor (s), I hereby declare that:

My residence, post office address and citizenship are as stated below next to my name.

I believe I am the original, first and sole inventor (if only one name is listed below) or an original, first and joint inventor (if plural names are listed below) of the subject matter which is claimed and for which a patent is sought on the invention entitled:

**METHOD FOR PROCESSING ERROR OF RECEIVED PACKET IN ETHERNET  
MACLAYER**

,the specification of which is attached hereto unless the following box is checked:

was filed on \_\_\_\_\_ as United States Application Number or PCT International Application Number \_\_\_\_\_ and was amended on \_\_\_\_\_ (if applicable).

I hereby state that I have reviewed and understand the contents of the above identified specification, including the claims, as amended by any amendment referred to above.

I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulation, § 1.56.

I hereby claim foreign priority benefits under Title 35, United States Code, § 119 of any foreign application(s) for patent or inventor=s certificate listed below and have also identified below any foreign application for patent or inventor=s certificate having a filing date before that of the application on which priority is claimed.

Prior Foreign Application(s)

1998-59204 (Number)	Republic of Korea (Country)	28/12/1998 (Day/Month/Year Filed)	Priority Claimed <input checked="" type="checkbox"/> Yes <input type="checkbox"/> No
_____ (Number)	_____ (Country)	_____ (Day/Month/Year Filed)	<input type="checkbox"/> Yes <input type="checkbox"/> No

I hereby claim the benefit under Title 35, United States Code, §120 of any United States application(s) listed below and, insofar as the subject matter of each of the claims of this application is not disclosed in the prior United States application in the manner provided by the first paragraph of the Title 35, United States Code, §112, I acknowledge the duty to disclose information which is material to patentability as defined in Title 37, Code of Federal Regulation, §1.56 which occurred between the filing date of the prior application and the national or PCT international filing date of this application.

(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)
(Application Number)	(Filing Date)	(Status - patented, pending, abandoned)

JC525 U.S. PTO  
09/473846

12/28/99

**POWER OF ATTORNEY:** I hereby appoint the following attorney(s) and/or agent(s) to prosecute this application and to transact all business in the Patent and Trademark Office connected therewith: Steve S. Cha, Registration No. 44,069; Howard S. Reiter, Registration No. 20,394.

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022491

PATENT TRADEMARK OFFICE

I (we) hereby declare that all statements made herein of my own knowledge are true and that all statements made on information and belief are believed to be true; and further that these statements were made with the knowledge that willful false statements and the like so made are punishable by fine or imprisonment, or both, under Section 1001 of Title 18 of the United States Code and that such willful false statements may jeopardize the validity of the application or any patent issued thereon.

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**Date:** December 28, 1999

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**Residence Address:**

**Post office address:** Same as above  
**Citizenship:** Republic of Korea

**Date:** \_\_\_\_\_

**Signature:** \_\_\_\_\_

**Full name of fourth inventor:**  
**Residence Address:**

**Post office address:** Same as above  
**Citizenship:** Republic of Korea  
**Date:** \_\_\_\_\_

**Signature:** \_\_\_\_\_